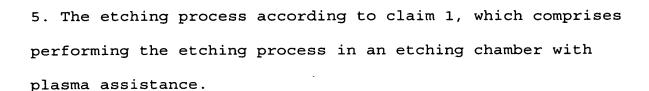
## I Claim:

1. In a dual damascene patterning process, an etching method which comprises:

providing a semiconductor structure with functional elements formed in a substrate, a dielectric disposed on the substrate, a photoresist etching mask above the dielectric, and a polymer intermediate layer between the etching mask and the dielectric layer;

etching the dielectric layer and the polymer intermediate layer for the dual damascene patterning with a CF4 ARC open process with high selectivity with respect to the photoresist of the etching mask.

- 2. The etching process according to claim 1, wherein the dielectric is an oxide layer.
- 3. The etching process according to claim 1, which comprises setting an etching time to at least twice an etching time of an  $O_2/N_2$  ARC open process.
- 4. The etching process according to claim 3, which comprises setting the etching time, depending on an etching depth, to approximately 140 s.



- 6. The etching process according to claim 5, which comprises etching with an RF power of approximately 600 watts.
- 7. The etching process according to claim 1, which comprises assisting the  $CF_4$  ARC open process by a proportion of  $CHF_3$ .
- 8. The etching process according to claim 7, which comprises setting a CF<sub>4</sub> flow during the ARC open process to approximately 40 sccm and setting the CHF<sub>3</sub> flow to approximately 20 sccm.
- 9. An etching process for oxide patterning in a semiconductor structure, which comprises:

providing a substrate with functional elements formed therein, an oxide layer on the substrate, an etching mask formed of a photoresist above the oxide layer, and a polymer intermediate layer forming an antireflection layer between the etching mask and the oxide layer;

patterning the oxide layer during a dual damascene patterning for a metallization;

etching the polymer intermediate layer and the oxide layer in a common  $CF_4/CHF_3$  etching process with high selectivity with respect to the photoresist; and

thereby adjusting an etching gas flow for  $CF_4$  to 35 - 45 sccm and an etching gas flow for  $CHF_3$  to 17 - 23 sccm in the common etching process.

- 10. The etching process according to claim 9, which comprises setting the etching time, depending on an etching depth, to approximately 140 s.
- 11. The etching process according to claim 9, which comprises performing the etching process in an etching chamber with plasma assistance.
- 12. The etching process according to claim 11, which comprises etching with an RF power of approximately 600 watts.
- 13. The etching process according to claim 9, which comprises setting the etching gas flow for  $CF_4$  to approximately 40 sccm and the etching gas flow for  $CHF_3$  to approximately 20 sccm in the common etching process.
- 14. The etching process according to claim 9, which comprises adding oxygen and argon to the etching gases, and setting a





gas flow of argon to 80 - 120 sccm and a gas flow of oxygen to 5 - 7 sccm.